Amendments to the Claims:

1. (Currently amended) A ~~temperature independent~~ CMOS reference voltage circuit, comprising:

a ~~CMOS~~ current mirror circuit ~~containing~~ comprising first and second ~~CMOS~~ transistors of a first polarity; ~~and~~

a temperature compensation circuit coupled to said ~~CMOS~~ current mirror circuit, ~~and containing a first resistor, a second resistor, and~~ comprising third and fourth ~~CMOS~~ transistors of a second polarity having current paths coupled respectively to current paths of the first and second transistors, a first resistor coupled to the current path of the third transistor opposite the first transistor, and a second resistor coupled between the current paths of the second and fourth transistors.

2. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said third and fourth ~~CMOS~~ transistors are configured to operate substantially in a subthreshold region.

3. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein one of said third and fourth ~~CMOS~~ transistors is diode connected.

4. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said fourth ~~CMOS~~ transistor is diode connected.

5. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein at least one of said first and second resistors is variable.

6. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said first resistor is coupled between ~~sources of said third and fourth CMOS transistors~~ the source of the third transistor and a voltage supply terminal.

7. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein gates of said third and fourth ~~CMOS~~ transistors are interconnected.

8. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein:

a first side of said second resistor is coupled to a drain of said fourth ~~CMOS~~ transistor; and

a second side of said second resistor is coupled to ~~said CMOS current mirror circuit~~ a drain of said second transistor for generating a reference voltage substantially unaffected by temperature changes.

9. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said temperature compensation circuit is configured to generate a reference voltage containing a proportional to absolute temperature (PTAT) voltage component and a threshold voltage of said fourth ~~CMOS~~ transistor.

10. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 9, wherein said PTAT voltage component and said threshold voltage have complementary temperature coefficients.

11. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 9, wherein said PTAT voltage component has a positive temperature coefficient and said threshold voltage has a negative temperature coefficient causing the reference voltage to be substantially unaffected by temperature changes.

12. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 11, wherein said positive temperature coefficient is proportional to kT/q.

13. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said first and second ~~CMOS~~ transistors are PMOS transistors and said third and fourth ~~CMOS~~ transistors are NMOS transistors.

14. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said first and second ~~CMOS~~ transistors are NMOS transistors and said third and fourth ~~CMOS~~ transistors are PMOS transistors.

15. (Currently amended) The ~~temperature independent~~ CMOS reference voltage circuit according to claim 1, wherein said ~~CMOS~~ current mirror circuit is configured as one of a cascode circuit and a gain boosted circuit.

16. (Currently amended) A CMOS temperature compensation circuit, comprising:

first and second ~~CMOS~~ transistors having interconnected gates and configured to operate substantially in a subthreshold region, said second ~~CMOS~~ transistor being diode connected;

a first resistor coupled between sources of said first and second ~~CMOS~~ transistors; and

a second resistor having a first end coupled to drain of said second ~~CMOS~~ transistor and having a second end coupled to a current mirror circuit for generating a reference voltage that is substantially unaffected by temperature changes.

17. (Original) The CMOS temperature compensation circuit according to claim 16, wherein said first resistor and said second resistor are variable.

18. (Currently amended) The CMOS temperature compensation circuit according to claim 16, wherein the reference voltage contains a proportional to absolute temperature (PTAT) voltage component and a threshold voltage of said second ~~CMOS~~ transistor.

19. (Original) The CMOS temperature compensation circuit according to claim 18, wherein said PTAT voltage component and said threshold voltage have complementary temperature coefficients.

20. (Original) The CMOS temperature compensation circuit according to claim 19, wherein said PTAT voltage component has a positive temperature coefficient and said threshold voltage has a negative temperature coefficient causing the reference voltage to be substantially unaffected by temperature changes.

21. (Original) The CMOS temperature compensation circuit according to claim 20, wherein said positive temperature coefficient is proportional to kT/q.

22. (Currently amended) The CMOS temperature compensation circuit according to claim 16, wherein said first and second ~~CMOS~~ transistors are NMOS transistors.

23. (Currently amended) The CMOS temperature compensation circuit according to claim 16, wherein said first and second ~~CMOS~~ transistors are PMOS transistors.

24. (Currently amended) An integrated ~~temperature independent CMOS~~ reference voltage circuit, comprising:

a substrate having a ~~CMOS~~ current mirror circuit ~~containing~~ comprising first and second ~~CMOS~~ transistors of a first polarity; and

a temperature compensation circuit coupled to said ~~CMOS~~ current mirror circuit, and ~~containing~~ comprising a first resistor, a second resistor, and third and fourth ~~CMOS~~ transistors of a second polarity, wherein the first resistor is coupled to a current path of the third transistor opposite the current mirror circuit, and wherein the second resistor is coupled between the second and fourth transistors.

25. (Currently amended) An integrated CMOS temperature compensation circuit, comprising:

a substrate having first and second ~~CMOS~~ transistors with interconnected gates and configured to operate substantially in a subthreshold region, said second ~~CMOS~~ transistor being diode connected;

a first resistor coupled between sources of said first and second ~~CMOS~~ transistors; and

a second resistor having a first end coupled to drain of said second ~~CMOS~~ transistor and having a second end coupled to a current mirror circuit for generating a reference voltage that is substantially unaffected by temperature changes.